

Korean International Semiconductor Conference & Exhibition on Manufacturing Technology 2025

## **KISM 2025 BUSAN**

Re:Innovation of Semiconductor Manufacturing for AI Ecosystem



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Staff Process Engineer at Applied Materials, Santa Clara, specializing in Chemical Mechanical Planarization (CMP) process and product development for advanced logic, memory, and packaging technologies. Focused on enabling next-generation AI and semiconductor devices, the work involves developing innovative CMP solutions such as 3D-printed pads and integrated endpoint detection technologies. Holds a Ph.D. in Chemical Engineering from Clarkson University, mentored by Prof. S. V. Babu, and has authored multiple publications along with several U.S. patents on advanced CMP pad design. Also served as a Guest Editor for the ECS Focus Issue "Chemical Mechanical Planarization (CMP): Past, Present, and Future)," and is an active peer reviewer for leading journals in semiconductor processing.