

# **KISM 2025 BUSAN**

Re:Innovation of Semiconductor Manufacturing for AI Ecosystem



## **Professor Changhwan Choi**

(Hanyang University, Korea)

#### [Education]

- · B.S, Materials Science and Engineering, Hanyang University, 2000
- · M.S, Materials Science and Engineering, The University of Texas at Austin, 2002
- · Ph.D, Electrical and Computer Engineering, The University of Texas at Austin, 2006 [Dissertation: The effects of Si, N and O incorporation and oxygen-scavenging technique on performance of Hf-based gate dielectric MOSFETs (Advisor: Jack C. Lee)]

#### [Work Experience]

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· 2010 - current	Professor, Materials Science & Engineering, Hanyang University
	Professor, Nanoscale Semiconductor Engineering, Hanyang University
	Professor, Semiconductor Engineering, Hanyang University
· 2024 - current	Head Professor & Director, Semiconductor Specialized Graduate School,
	Hanyang University
· 2019 - current	Director, Industrial Materials and Technology Research Center, Hanyang
	University
· 2023 - current	Advisory Professor, Logic Semiconductor Technology, Samsung
	Electronics R&D Center
· 2023 - 2024	Visiting Professor, Microelectronics Research Center, The University of
	Texas at Austin, Austin, TX, USA
· 2016 - 2017	Visiting Professor, Center for Spintronics, Post-Silicon Semiconductor
	Institute, Korea Institute of Science and Technology (KIST)
· 2006 - 2010	Research Staff Member, IBM Thomas J. Watson Research Center,
	Yorktown Heights, NY, USA

### [Research Interests]

- · ALD HKMG-based Advanced Logic & Memory Device & Process (i.e, ALD High-K Gate Dielectric, Metal Gate, Oxide Semiconductor, Si-based Thin film, AS-ALD/ALE, Post-Metallization Metal/Dielectrics, Metal Contacts/Barrier etc)
- · Ferroelectric Thin Film-based Device & Process (i.e, FeFET, FeRAM, FTJ, FE-VNAND Flash Memory etc)
- · Neuromorphic Device, Process & System (i.e., 2-terminal & 3-terminal based Devices for Artificial Synaptic Device & Array System etc)
- · 3D Heterogeneous Integration Device & Process (i.e, Monolithic & Sequential 3D Process etc)
- · Advanced Semiconductor Packaging Materials & Process (i.e., Wafer Bonding, RDL, TGV, Electroplating, Build-up Materials, High Thermal Conductivity Materials, Signal Integrity etc)