

Korean International Semiconductor Conference & Exhibition on Manufacturing Technology 2025

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Re:Innovation of Semiconductor Manufacturing for AI Ecosystem



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Jiho Kang, Ph.D. is the Vice President in SK hynix, currently leading Cleaning and CMP (including Wafer Bonding) process development in R&D Division.

Prior to joining SK hynix, Dr. Kang joined Intel Corporation in Hillsboro, Oregon in 2006 and worked as a senior etch process engineer. From 2012, he participated in the development of Intel TSV process technology, which became the basis of Intel Foveros[™] Technology. From 2016, he worked as a group leader, responsible for BEOL process development for Intel 14, 10 & 7nm technology nodes.

Dr. Kang received Ph.D. in Materials Science and Engineering from The Ohio State University, Columbus, Ohio. Previously, he earned B.S. in the Metallurgical Engineering from Yonsei University and M.S. degree in Materials Science and Engineering from KAIST in Korea.